ABSTRACT OF THE DISCLOSURE

One embodiment of a distributed memory module cache includes tag memory and associated logic implemented at the memory controller end of a memory channel. The memory controller is coupled to at least one memory module by way of a point-to-point interface. The data cache and associated logic are located in one or more buffer components on each of the memory modules. This embodiment includes an option to segment the cache. When the cache is segmented, the cache line size is halved. The segmentation allows the entire cache to be accessed without doubling the amount of tag address storage locations. The non-segmented cache may be used for memory systems using a burst length of eight bytes, while the segmented cache may be used for memory systems using a burst length of four bytes.